SYSTEMS PRODUCTS
LOGICAL PRODUCTS
PHYSICAL IMPLEMENTATION
SIMULATION AND ANALYSIS
LIBRARIES
TCAD

Aurora
DFM WorkBench
Davinci
Medici
Raphael
Raphael-NES
Silicon Early Access
TSUPREM-4
Taurus-Device
Taurus-Lithography
Taurus-OPC
Taurus-Process
Taurus-Topography
Taurus-Visual
Taurus-WorkBench

DFM WorkBench

Design for Manufacturability Solutions

DFM WorkBench bridges the gap between process development and circuit design by allowing semiconductor engineers to account for statistical variations in the process to improve circuit performance, maximize wafer yield and reduce time to volume production. Statistical modeling through factory emulation using TCAD simulators makes it possible to take design for manufacturability into consideration even before running real silicon wafers. By using Monte Ca sampling, a virtual pilot line is generated in the computer. DFM WorkBench provides a simulati environment to obtain early SPICE models for circuit designers and statistical information for yi enhancement.

DFM WORKBENCH BENEFITS

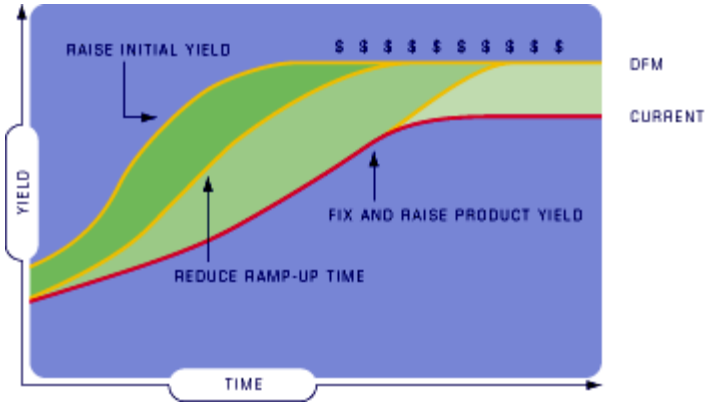
- **Generates "Early SPICE" models for circuit simulation:**
  - - Performs Monte Carlo sampling on process and device simulation.
  - - Extracts SPICE model parameters (e.g. BSIM3 v3 or BJT Gummel-Poon).
  - - Creates fast and slow SPICE models.

- **Improves product performance and yield:**
  - - Correlates process statistical variations with circuit performance.
  - - Performs process diagnosis.
  - - Sets statistical process control limits.
  - - Predicts yield based on statistics.

- **Reduce development time and cost.**

DESIGN FOR MANUFACTURABILITY

The task of developing advanced IC manufacturing processes has become extremely complex objective of DFM WorkBench is to enable IC manufacturers to maximize their return on investn through cost reduction, cycle time reduction and yield maximization. The figure to the right depi how DFM WorkBench can help maximize product yield at various stages of product life. In the process development stage (first curve), statistical information generated from simulation-base experiments allows circuits to be designed for manufacturing, thus raising the product's initial yi During pilot line manufacturing (middle curve), understanding the behavior of the product in a manufacturing environment through simulation allows engineers to reduce ramp-up time by optimizing the integrated process. For a production process (last curve), the ability to quickly ide the cause of yield failures and make corrections using simulation results is crucial to raising the product yield to its maximum potential.



DFM WorkBench helps maximize product yield at various stages of product life.

DFM WORKBENCH DESCRIPTION

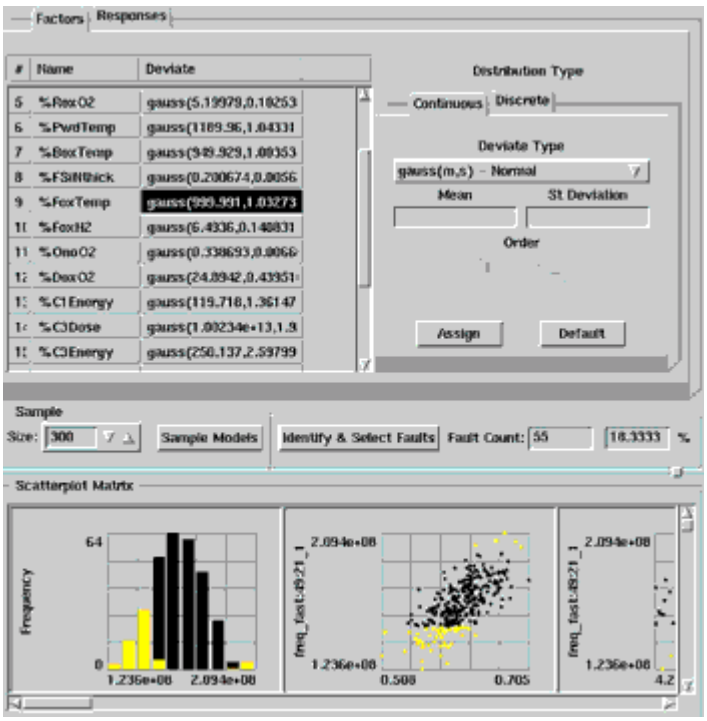
DFM WorkBench is a productivity enhancement tool that lets engineers perform statistical mod and yield analysis through simulation-based experiments.

DFM WorkBench takes the nominal process flow optimized in Taurus WorkBench as the basel process. With the process variation statistics, Monte Carlo sampling is performed on the nomin process using physical process and device simulations. DFM WorkBench automatically sets up necessary split runs and manages the simulations. Users have the choice of extracting SPICE, generating look-up tables for Star-Sim for subsequent circuit simulations. The outputs can be u to generate statistical SPICE models including skew model generation, perform process diagnostics, optimize product performance and predict yield. Thus, "Early SPICE" models can b made available to circuit designers even before silicon is run.

With DFM WorkBench, circuits can be designed to account for statistical variations in the manufacturing process. The result is faster turnaround in the design and shorter time to volume production with a faster ramp to maximum potential yield.

ACCOUNTING FOR PROCESS VARIATIONS

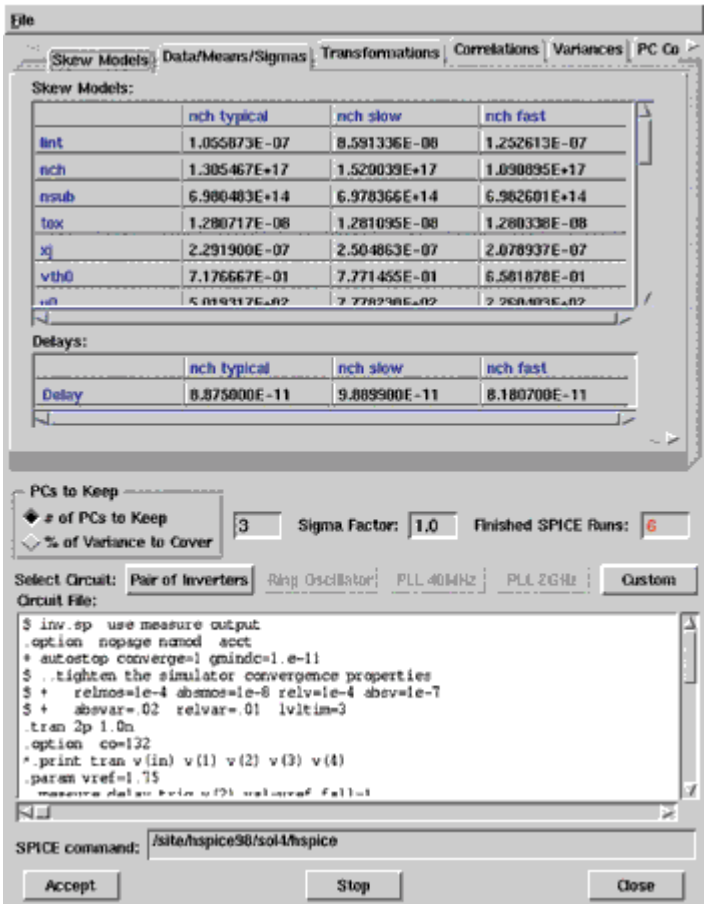
The figure to the right shows the process inputs and the electrical responses. Such distributions provide statistical information for optimizing device performance and correlating circuit performa with process statistics.



Output electrical distribution

PERFORMANCE ANALYSIS TOOL

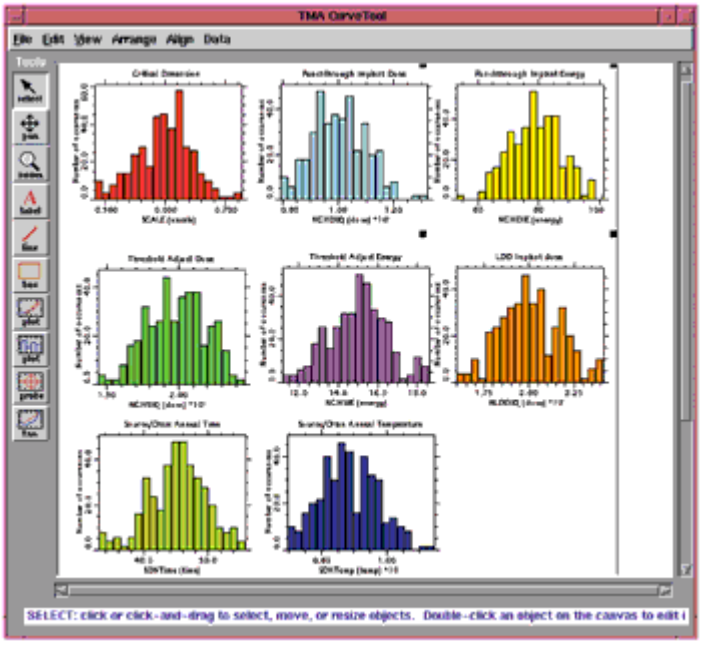
Monte Carlo Sampling using Response Surface Methodology (RSM) can promptly generate ne distributions without rerunning process and device simulations. The Performance Analysis Tool (PAT) automatically reports the device or circuit performance distribution in histogram and scat plots, highlighting the "out-of-spec" items (yellow). By simply varying the value of mean and sig of key process parameters, new distributions and the fault count, showing out-of-spec items are estimated by Monte Carlo sampling on RSM. PAT makes it easy to predict yield from the statist information.

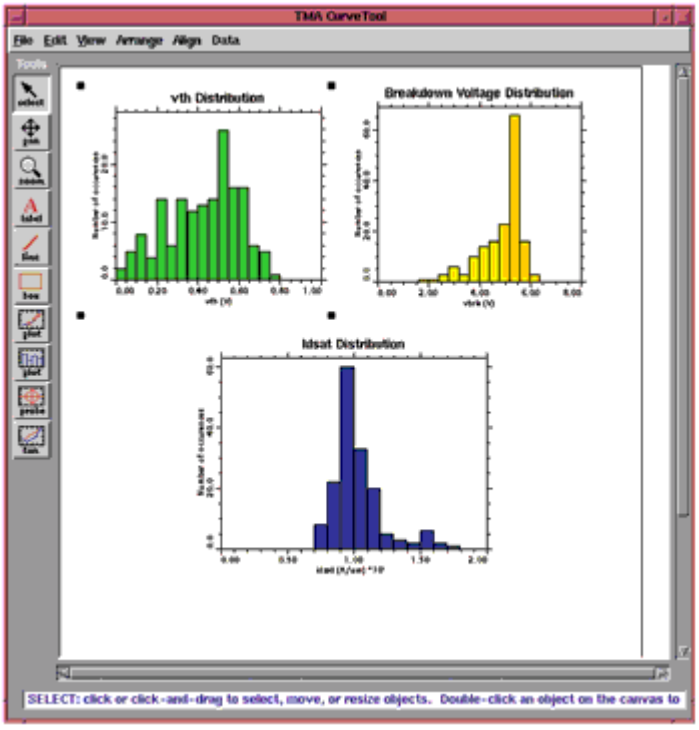


Performance Analysis Tool provides a snapshot of device and circuit performance.

SKEW MODEL GENERATOR

Using SPICE parameters extracted from statistical simulations, the Skew Model Generator crea a set of slow and fast SPICE model parameters by performing PCA (Principal Component Anal and analyzing the Eigen value. With skew models, a circuit designer can optimize the circuit to maximize its performance.





Skew Model Generator Window and simulated fast (red) and slow (blue) IV curves.

DFM WORKBENCH FACTS AND FEATURES

- Tight integration with Taurus WorkBench to import baseline flow.
- Flexible post-processing with user-defined macros and tools.
- Direct correlation between process parameters and circuit performance.
- Process: TSUPREM-4.
- Device: Medici.
- Layout: Taurus-Layout.
- Visualization: Taurus-Visual.
- Circuit Simulation: SPICE, Star-HSPICE, Star-Sim.
- SPICE Models: BSIM3v3, BJT Gummel-Poon.

Histogram distribution of SPICE parameters and circuit performance:

- Correlates circuit performance with process parameters.

Statistical BSIM3 and Gummel-Poon model parameters:

- Generates statistical models as inputs to circuit simulation.
- Provides distribution of circuit performance.
- Generates fast and slow models through Principal Component Analysis (PCA) or simple skews of user-specified parameters.

Look-up table for STAR-Sim:

- Generates look-up tables for circuit simulations with Star-Sim.

Yield analysis:

- Response surface modeling (RSM) and regression analysis.
- Monte Carlo sampling with RSM.
- Calculates statistical profiles.
- Performance Analysis Tool.

SYSTEM CONFIGURATION REQUIREMENTS
Platform: DFM WorkBench operates on UNIX workstations from Hewlett-Packard, IBM and Sur Microsystems.

Memory: 64 Mbytes.

Disk Space: 80 Mbytes for executable. Additional disk space is required for simulation data stor based on integrated tool set and application.
