

# On Impacts Of ESD Protection Structure On Circuit Performance In Aluminum And Copper Interconnects

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## ABSTRACT

This paper presents a comparison study on influences of on-chip electro-static discharge (ESD) protection structures on performance of the circuits protected, using 1.5V, 0.18 $\mu$ m aluminum and copper interconnect technologies, respectively. A low-power, high-speed Op Amp was designed. Simulation results show that while ESD parasitics may degrade the circuit performance inevitably, the use of Cu interconnects can substantially recover such corruption compared to using Al, while maintains better ESD protection.

## INTRODUCTION

Parasitic effects of on-chip ESD protection structures become significant issues in high-speed and RF IC design, as chip sizes continuously shrink. Similar to the well-known global interconnect timing issues, the parasitic capacitance,  $C_{ESD}$ , of ESD protection structures may corrupt circuit performance as well, such as, clock signals, band width, stability, etc. The problem becomes even more challenging these days as the marketing strategies drive ESD specification level higher and higher, leading to ever-larger size for

ESD structures, therefore even more ESD parasitic effects. On the other hand, it is reported that new copper interconnect technology delivers many benefits to IC designs as compared to its aluminum counterpart, *e.g.*, higher speed, better reliability in terms of both electromigration harness and ESD robustness<sup>[1]</sup>. However, little has been reported regarding how seriously ESD structures may affect the circuits protected and how well the copper technology may alleviate this problem. Such problem was studied in this work.

## DESIGN

In this work, a low-power, high-performance Op Amp circuit with CMOS-type ESD protection was designed in 0.18 $\mu$ m aluminum and copper interconnect technologies. Comprehensive studies were then conducted to estimate how much parasitic  $C_{ESD}$  exists, to investigate how seriously  $C_{ESD}$  may deteriorate the Op Amp performance, such as speed, driving capability and stability, etc. as well as to demonstrate how well the Cu ESD design may recover such degradation. The design uses the commercial 1.5V, 0.18 $\mu$ m one-poly, six-

metal Cu and Al high-speed CMOS technologies from the UMC foundry.

### A. ESD Protection

In order to illustrate the interactions between ESD structures and the core IC circuits, this design chose to use the conventional ground-gate CMOS (GGMOS) ESD protection structure <sup>[2]</sup> because of its ubiquitousness and large size. The target ESD protection level is 4kV to reflect current market trend. The schematic of a GGMOS ESD structure and a complete ESD protection scheme are shown in *Fig 1*. In principle, the normally off ESD units are triggered on during an ESD event to form a low-impedance discharging path to shunt the huge transient ESD pulses, therefore protect the core circuit against ESD damages. For comparison purpose, two versions of ESD structures and circuits were designed using Cu and Al interconnects, respectively. To ensure meaningful comparison between Cu and Al designs, the same ESD compliance level (4KV) were used for both ESD chips. ESD simulation<sup>[3, 4]</sup> was performed to predict the ESD performance as well as to guide the size selection of the ESD devices for adequate ESD performance. The simulation shows that to achieve the same ESD protection level, over 30% of metal width reduction can be obtained in using Cu interconnects as compare to using the conventional Al interconnects. This substantial size reduction translates into significant decrease of the parasitic ESD capacitance  $C_{ESD}$ , to be discussed in the following sections.

### B. Estimation of Parasitic $C_{ESD}$

According to the design rules, metal layers 1 and 2 were used in ESD design where metal 1 layer (M1) was used for

primary ESD metal and metal 2 (M2) was used for interconnect bridges. Study of the layout shows that the main source of ESD parasitic capacitance,  $C_{ESD}$ , comes from the ESD metal line associated inter-layer capacitance, including metal-to-substrate, inter-metals, as well as metal-to-poly-gate. Therefore, the total  $C_{ESD}$  consists of the following capacitances: M1-to-substrate, M1-to-Diffusion, M1-to-Poly 1, and M1-to-M2. Material data for inter-layer dielectric thickness and permittivity ( $\epsilon$ ) that were used to calculate the  $C_{ESD}$  is listed in *Table I*. In calculating  $C_{ESD}$ , parasitic capacitance from both NMOS and PMOS ESD units are included based upon the complete ESD protection topology shown in *Fig. 1*. The estimated data for  $C_{ESD}$  are summarized in *Table II*, which shows substantial parasitic capacitance from the ESD structures and roughly 30% of  $C_{ESD}$  reduction for the Cu ESD circuit as compared to the Al version.

Table I Inter-layer dielectric thickness and permittivity data for  $C_{ESD}$  estimation

From	To	Thickness (KÅ)
Metal 1	Diffusion	10
Metal 1	Sub-strate	14
Metal 1	Poly-1	8
Metal 1	Metal 2	5.7
ILD-layers	ILD-films	$\epsilon$
STI	SiO2	3.6
ILD	Si3N4	7
MD1	SiO2	3.6

Table II Estimated  $C_{ESD}$  for 4KV GGMOS

GGMOS	Cu	Al
Full-ESD $C_{ESD}$ (pF)	0.300	0.429

### C. Op Amp Circuit

To illustrate the whole-scale influences of the ESD parasitic  $C_{ESD}$  on the circuits, a low-power, high-performance Op Amp is designed and used as a test vehicle in this work. The Op Amp design targets include low power, high slew rate, short settling time, wide output swing and large bandwidth. The circuit schematics are shown in *Fig. 2*, which has the following features: A differential pair input stage for better noise rejection; a source-follower gain stage for high gain as well as level shift; A class AB complementary push-pull output stage with low quiescent current for high-swing, low power consumption, as well as crossover distortion elimination; and a compensation capacitor  $C_C$  with active nulling resistor for wide band width and adequate stability.

## SIMULATION AND DISCUSSION

### A. Op Amp Performance

The Op Amp circuit operates at  $V_{DD}=1.5V$ . SPICE simulation was performed for both stand-alone Op Amp circuits and the circuits with  $C_{ESD}$  included to represent the parasitic ESD capacitive effects. The simulation data for the stand-alone Op Amp circuit are summarized in *Table III*, which shows very low power consumption of 0.47 mw; gain of 74dB, phase margin of  $62^\circ$ ; unity-gain band-width of 156 MHz; wide output swing of 0.96V (measured at 80% small-signal gain), very high slew-rate of 215 mV/ns; and very short settling time of 5 ns measured at 1% of the output. External load ( $C_L$ ) of 1 pF is used for data extraction.

### B. Performance Comparison

Simulation with different  $C_{ESD}$  for both Cu and Al interconnects was conducted

for the purpose of comparison. The typical circuit performance are shown in *Figs.3-6* for the gain Bode plot, phase Bode plot, large-signal step response for slew-rate test and small-signal step response for settling time extraction. The typical circuit specification data are extracted and summarized in *Tables IV & V* for comparison study. The results clearly show that parasitic ESD capacitance may substantially corrupt the circuit performance, for example, over 20% reduction in bandwidth, 15% decrease in slew rate and 57% increase in settling time. The data also demonstrate that, while maintaining the same ESD protection level, the use of Cu interconnects can significantly alleviate such circuit performance deterioration, *e.g.*, ~20% recovery over a broad range. It is therefore beneficiary to use Cu interconnect technology in high-speed IC designs.

Table III. The Op Amp circuit specifications

Technology	0.18um, 1.5V, Cu, 1P6M
Power supply (V)	1.5
Gain (dB)	74.21
Phase margin	$62.2^\circ$
$f_T$ (MHz)	156.5
$f_{.3dB}$ (kHz)	33.9
V-swing (V, @80%)	0.96
Settling time (ns, @1%)	5.01
SR (mV/ns)	215.6
Power cons. (mw)	0.469

Table IV. Influences of  $C_{ESD}$  loads on the Op Amp circuit: Cu ~ Al, ( $C_L = 1pF$ ).

ESD	$C_{ESD}$ (pF)	$f_T$ (MHz)	Phase marg.	SR (mV/ns)	$t_{set}$ (ns)
None	0	156.5	$62.2^\circ$	215.6	5.01
Al	0.3	118.8	$59.9^\circ$	181.8	7.88
Cu	0.43	127.4	$60.8^\circ$	190.7	7.28

## CONCLUSION

In summary, a comparison study was conducted to investigate the influences of on-chip ESD protection structures on performance of the circuits protected, using aluminum and copper interconnect technologies, respectively. Simulation results show that parasitic ESD effects may degrade the circuit performance substantially and inevitably. It also demonstrates that the use of Cu interconnects can substantially alleviate such corruption problem as compared to using Al interconnects, while maintaining the same or better ESD performance.

Table V. Op Amp performance degradation due to  $C_{ESD}$  loads: Cu ~ Al.

Parameters	No $C_{ESD}$	Al	Cu
$f_T$ (MHz)	156.5	-24.1%	-18.6%
		Reduction in Degradation	
		→ +22.8% →	
Phase Margin	62.2°	-3.7%	-2.3%
		Reduction in Degradation	
		→ +39.2% →	
Slew rate (V/us)	215.6	-15.7%	-11.5%
		Reduction in Degradation	
		→ +26.8% →	
$t_{set}$ (ns, 1%)	5.01	-57.3%	-45.3%
		Reduction in Degradation	
		→ +20.9% →	

## ACKNOWLEDGEMENT

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## REFERENCES

1. S. Voldman, *et al.*, "High-current TLP characterization of Al and Cu interconnects for advanced CMOS semiconductor technologies", in *Proc. of Int'l Rel. Phys. Symp.*, pp.293-301, 1998.
2. A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, John Wiley, New York, 1995.
3. A. Wang and C. Tsay, "A Novel Design Methodology Using Simulation For On-Chip ESD Protection For ICs", *In Proc. of IEEE 5<sup>th</sup> Int'l Conf. Solid-State IC Technology*, pp.509-512, 1998.
4. A. Wang, H.G. Feng and K. Gong, A SRC Cu Design Contest Report, 1999.

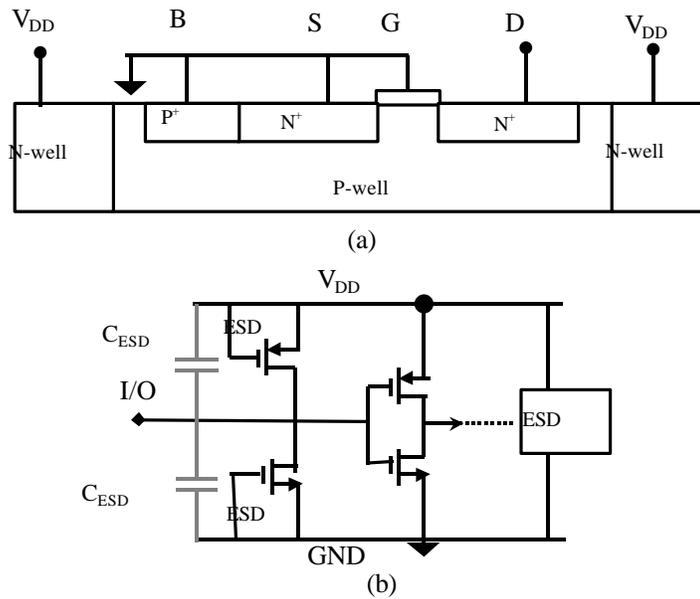


Fig. 1 GGMOS ESD protection structure: a) cross-section for a GGMOS, b) a complete ESD protection scheme.

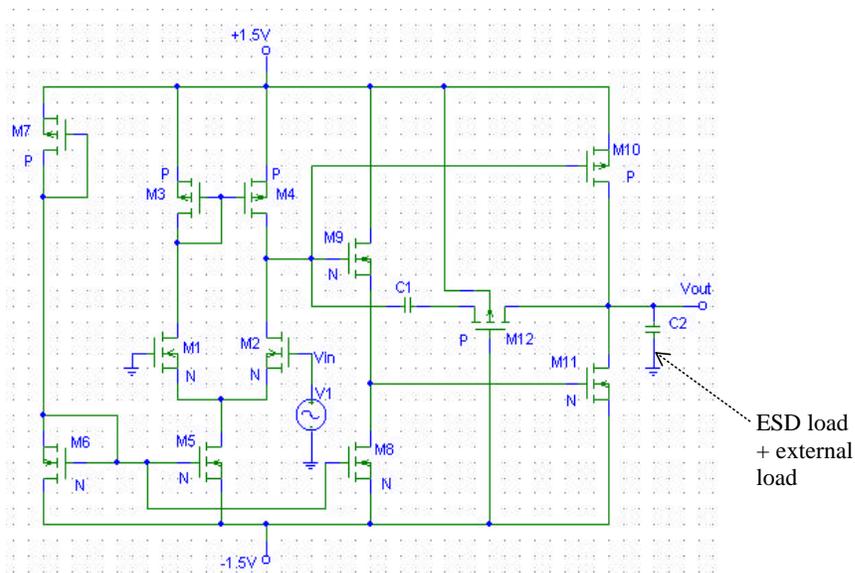


Fig. 2 Schematic of a high-performance Op Amp circuit. Parasitic capacitive side effects from ESD protection units are simulated by  $C_{ESD}$  connected to the I/O pins.

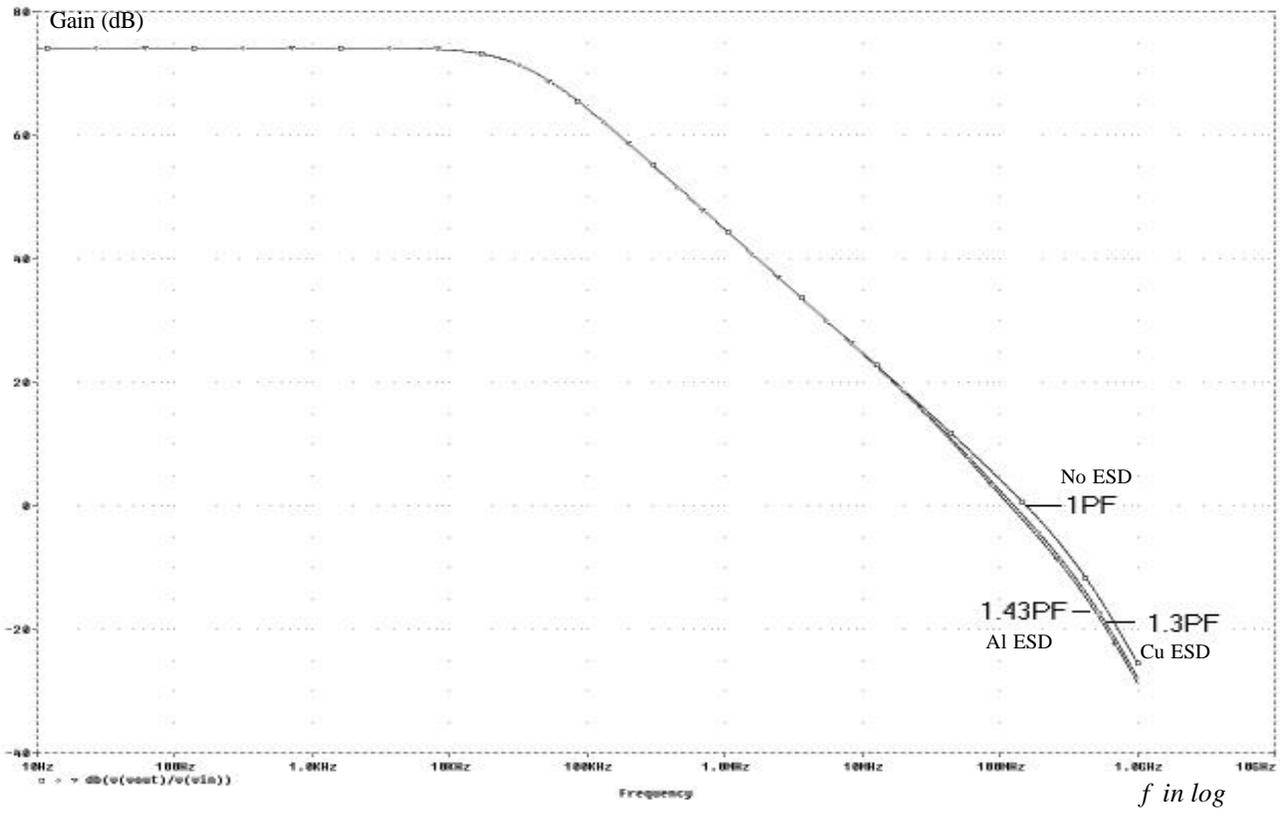


Fig. 3 Gain plot of the Op Amp circuit with  $C_{ESD}$  load.

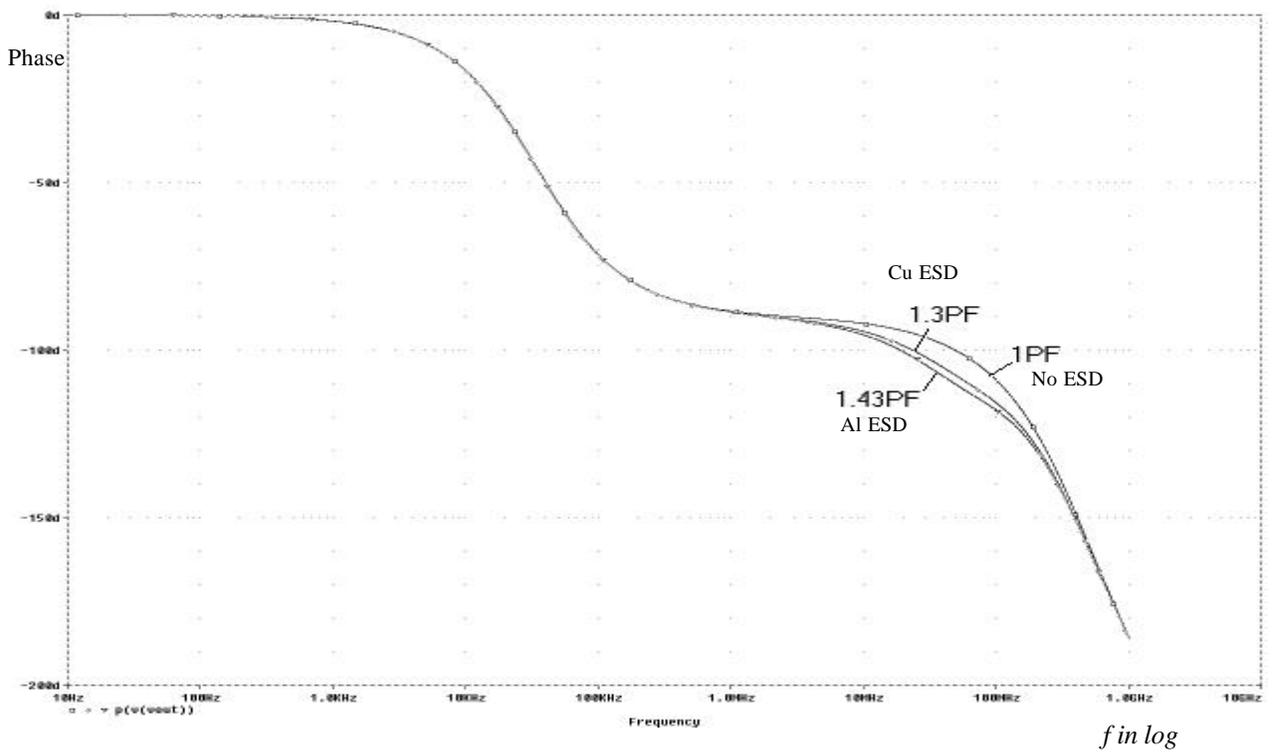


Fig. 4 Phase plot of the Op Amp circuit with  $C_{ESD}$  load.

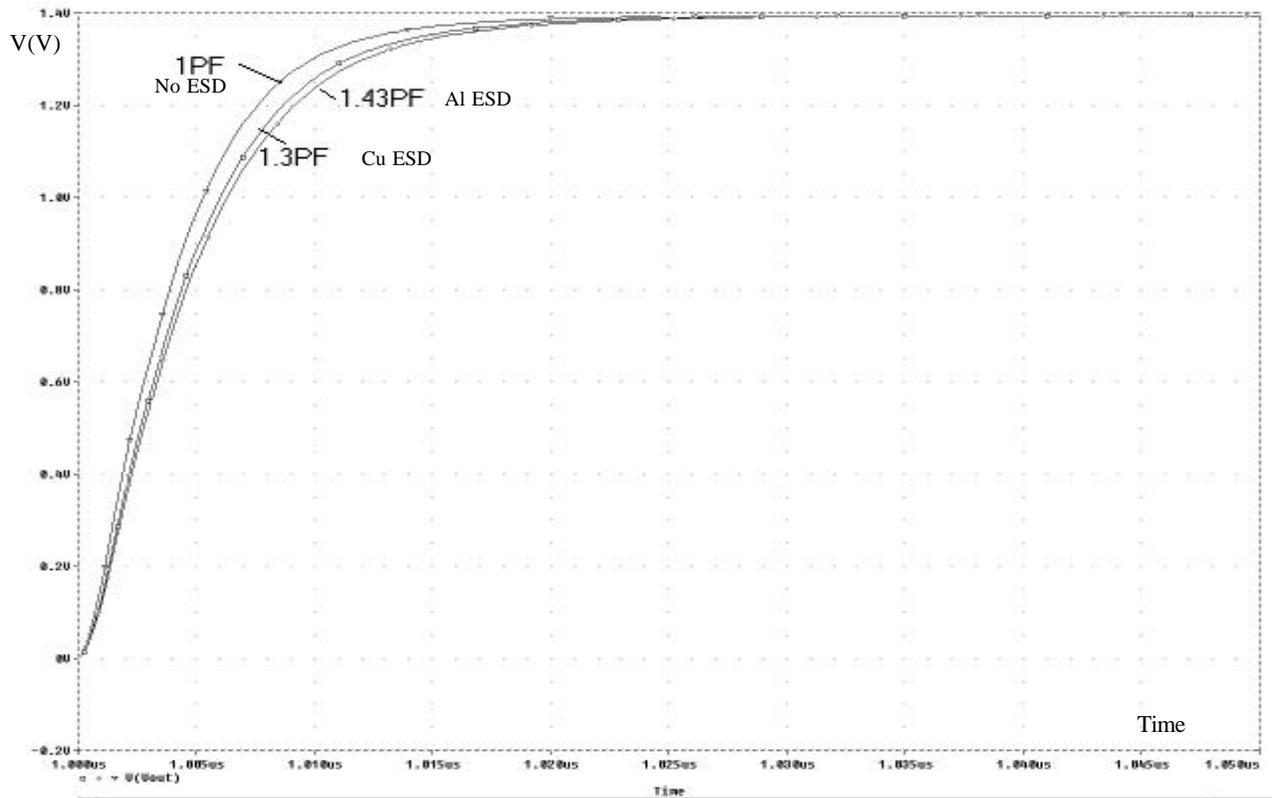


Fig. 5 Large-signal step response plot of the Op Amp circuit with  $C_{ESD}$  load for slew-rate test.

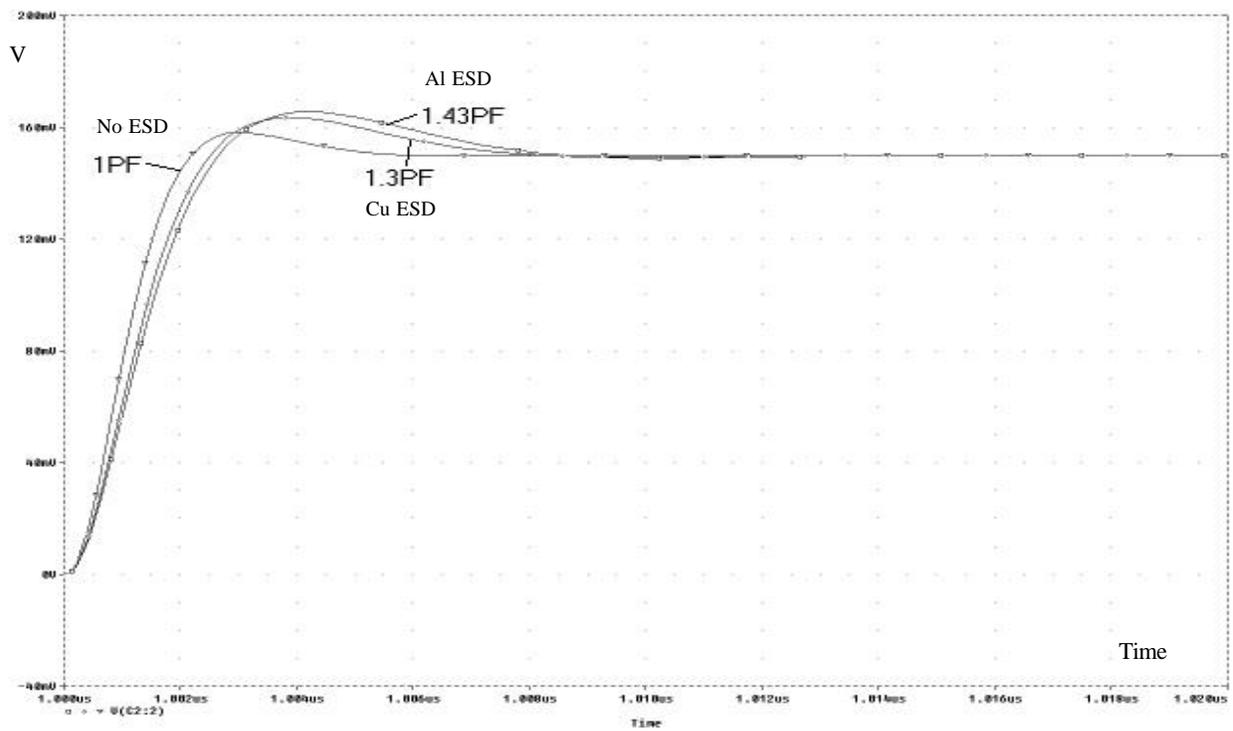


Fig. 6 Small-signal step response plot of the Op Amp circuit with  $C_{ESD}$  load for settling-time test.