ESD-Induced Circuit Performance Degradation in RFICs

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Abstract

ESD structures have inevitable parasitic impacts on circuit performance. This paper reports results of an investigation into ESD-induced circuit performance degradation in RFICs including clock corruption, reduced slew rate, narrowed bandwidth, and noise generation. Performance degradation of ~80%, ~30% & ~5% were observed in clock, Op Amp and LNA circuits studied, which were recovered substantially by using novel compact ESD structures that are critical to reducing ESD influences on circuits while maintaining adequate ESD performance.

Introduction

ESD protection for RFIC applications is becoming a new design challenge because of the substantial interactions between the ESD protection structures and the circuits protected. On one hand, the circuit-to-ESD influences exit that often leads to premature ESD failures – a well-studied ESD topic. On the other hand, the ESD-to-circuit influences are inevitable, which may substantially degrade circuit performance. This under-studied topic gets more attention in RF and VDSM IC design recently. The main ESD-to-circuit impacts include RC effect of ESD-induced capacitance (C_{ESD}) and ESD-related noises. Such ESD-induced parasitic effects become intolerable to high frequency applications. Considering that a complete ESD protection solution requires multiple ESD devices for each I/O pin to against ESD pulses of all modes: *i.e.*, I/O-to-V_{DD} positively (*PD*) & negatively (*ND*), I/O-to-ground (GND) positively (*PS*) & negatively (*NS*), and power clamps [1, 2], the overall ESD-induced parasitic might substantially corrupt the circuit performance. It is imperative to develop novel compact ESD protection structures with low ESD parasitics for high-frequency applications. In this work, ESD-to-circuit influences of different ESD devices on several RF IC chips, *e.g.*, a GHz ring-oscillator, a high-performance Op Amp, and a low noise amplifier (LNA) circuit, were investigated.

ESD Design and Measurements

This work compares the conventional MOS ESD structure (ESD*1*) with two new ESD structures (ESD*2* & ESD*3*)[2, 3] for the same ESD performance level, ESDV = 4KV HBM.

I. ESD1: MOS ESD structures

Fig. 1 illustrates a conventional MOS ESD structure. Normally, GGNMOS and GGPMOS devices are used to protect I/O pins against all ESD pulses (PD. ND, PS, & NS) as shown in *Fig.1a*. *Fig. 1b* is a typical NMOS cross-section showing parasitic junction capacitance. Only C_{gd} and C_{db} have effects in GGNMOS as modeled in *Fig. 1c*. Both NMOS and PMOS ESD structures contribute to the overall parasitic capacitance, C_{ESD}. From ESD simulation, four 200μm-wide NMOS fingers were needed for 4KV protection, as confirmed by HBM zapping. Simulation and measurement data match well as shown in *Table I*.

II. ESD2: A New Dual-Direction ESD Structure

Ideally, an ESD protection unit should provide low-impedance current shunting-channels formed by *active* devices in all ESD stressing modes. However, in the NMOS ESD structure, only one active discharging-path is formed by a NPN device, with a parasitic diode serving as a I-shunting path in the opposite direction that often limits the ESD performance, which cannot be used for V_{DD}>5V because 10% ΔV_{DD} may turn on the diode accidentally. A new dual-direction ESD structure (ESD2) [3] was designed to address this problem as illustrated in *Fig. 2*. Briefly, ESD2 is a two-terminal (A & K), five-layer ($N_1P_2N_3P_4N_5$) structure consists of one lateral PNP ($Q_1=P_2N_3P_4$), two vertical NPN ($Q_2=N_1P_2N_3$ & $Q_3=N_3P_4N_5$) and four parasitic resistors, R_1, R_2, R_3, & R_4. The structure forms two functional SCR units: unit 1= Q_1-Q_2 and unit 2= Q_1-Q_3. In operation, when a positive ESD pulse appears at *A* (*w.r.t. K*), *BC* junction (N_3P_4) of Q_1 is reverse biased to its breakdown and the generated holes are collected by the negative terminal *K* via P_4-P^+ layer. V_{BE} (P_4N_5) of Q_3 increases and eventually turns on Q_3. The SCR unit 1 is therefore triggered off (at V_{t1}) and driven into deep snapback region (holding voltage $V_h \leq 2V$). An *active* I-path with negligible R_{ON} is thereby formed to shunt ESD current and clamp the I/O pad voltage at V_h. After the ESD pulse is over, the thyristor is quickly discharged and then turned off when the current decreases to below its holding current level. Similarly, the SCR unit 2 operates during a negative ESD pulse event (*K w.r.t. A*). Hence this forms a dual -direction ESD protection device. Data from simulation and measurements are in *Table I*. A 50μm device passed HBM ESDV=4KV and a 200μm device passed 14KV (test limit). Compared to the MOS ESD1, the ESD2 features dual-polarity operation and smaller size. Therefore, ESD2 has much lower C_{ESD} as shown in *Table I*, which greatly reduces the capacitive effects on the circuits. However, two ESD2's are still needed for each I/O pin for I/O-to-V_{DD} and I/O-to-Gnd, respectively. In addition, one extra power clamp is needed. Hence sizable C_{ESD} still exists, especially for high-pin-count circuits.

III. ESD3: A New All-Direction ESD Structure

ESD3 is a new all-direction ESD protection structure [4] with three terminals (*A*, K_1, & K_2) and eight layers (N_1, P_2, N_3, P_4,

N_5, N_6, P_7, N_8) as illustrated in *Fig. 3a*. It consists of six bipolar transistors, which form two ESD2-type units. Unit I consists of Q_1, Q_2 & Q_3. Unit II has Q_4, Q_5 & Q_6. Q_3 and Q_5 share base and collector layers. A complete full-ESD protection scheme using ESD3 is shown in *Fig. 3b*. Operation of ESD3 is basically a dual-operation of ESD2 units. Its three electrodes, A, K_1 & K_2, are connected to I/O pin, V_{DD} and Gnd, respectively. During ESD events, when ESD pulses appear at I/O pin *w.r.t.* V_{DD} or GND, the Unit I or Unit II will function exactly the same way as the ESD2 does. ESD3 also operates symmetrically as shown by the measured I-V curve in *Fig. 4*. Typical data from simulation and tests are in *Table I*. A 50μm device was needed for 4KV. The major advantages of the ESD3 over the ESD2 are the following. First, *one* ESD3 device for each I/O pin can provide ESD protection against all four ESD pulsing modes: ND by path ①, PD by path ②, PS by path ③, and NS by path ④ as shown in *Fig. 3b*. Second, a similar ESD2-type SCR device exists between terminals K_1 and K_2, which forms a V_{DD}–clamp for DS pulse (I-path ⑤). Therefore, one single ESD3-type device is enough to provide complete ESD protection for each I/O. Third; it hence introduces much lower parasitic C_{ESD} as shown in *Table I*. In addition, ESD3 is suitable for bondpad-oriented ESD design and is layout friendly. Overall, ESD2 represents ~83% reduction in C_{ESD} compared to ESD1, while ESD3 further reduces C_{ESD} by ~ 22% over ESD2, therefore benefit circuits.

ESD C_{ESD} Impacts on RFICs

A GHz ring-oscillator and a high-speed Op-Amp were used to investigate the C_{ESD}–to-circuit impacts, implemented a 0.18μm 1.5V commercial CMOS technology.

I. Ring-Oscillator Clock Corruption

A 15-stage ring-oscillator circuit was designed running at 4.7 Ghz. Since overall C_{ESD} effect in practical circuits varies according to I/O pin counts, two ESD loading cases were considered in this work: a single-load scenario representing the least effect where only one I/O pin has ESD unit and a full-load scenario showing multi-pin ESD connection where ESD units were connected to each stage. The clock frequency data are listed in *Table II*. It is observed that C_{ESD} of ESD*1* dramatically reduced the clock speed (85% ~ 99%) for single-load and full-load cases, respectively. However, the new ESD structures can recover the corruption significantly, 41% for ESD2 and 62% for ESD3, respectively, in the single-load case.

II. Impacts on Hi-Performance Op-Amp Circuit

A low-power, high-speed, wide-swing Op Amp circuit, designed for wireless communication applications, was used to demonstrate the influences of parasitic C_{ESD} on overall performance of a functional chip. The circuit features differential input, push-pull output stage for wide swing, level shift, capacitive compensation with nulling resistor for better stability, and global biasing for low-power, delivering very low power consumption of 0.4 mW, high unity-gain and -3dB band-width of 126MHz and 40 KHz, wide swing of 0.96V measured at 80% small-signal gain, very high slew-rate of 115 mV/nS, and short settling time of 9 nS measured at 1% of the output. C_{ESD} is connected to the output node to evaluate the negative impacts of ESD on the Op Amp performance. Data in *Table III* show substantial degradation in circuit performance due to ESD1, *i.e.,* ~ 30% deterioration in unity-gain bandwidth, slew rate and settling time, all critical in high-speed operation. ESD2&3 recover the performance corruption by 60 ~ 80% in this case.

ESD-Induced Noises

ESD structures contribute to the overall circuit noises in two ways. First, line noises may be coupled into the circuit more easily due to C_{ESD}. Second, self-induced noises by ESD units will deteriorate circuit noise performance, which was investigated in this work. Both effects are ESD-size related.

A LNA circuit with novel on-chip Cu inductors and transformers was designed for RF transceivers. Noise figure was obtained for the LNA without and with ESD protection. *Fig. 5* shows clearly that the NF value increases, as the ESD structure size gets bigger, indicating worse noise performance due to ESD-induced noises. Using different ESD protection structures for the same 4KV protection, *e.g.,* ESD1 (200um) and ESD2 (50um), resulted in different noise performance. In a case only one single GGNMOS (ESD1) or ESD2 were used for one I/O pin, the data in *Table IV* shows better noises performance for ESD2 case than ESD1 case. In practice, the noise performance might be even worse when using NMOS ESD because multiple ESD devices are needed for each I/O pin for complete protection. It is evident that novel compact ESD protection structures are critical to achieve adequate ESD protection while maintain low ESD-to-circuit influences.

Conclusions

In summary, ESD-to-circuit influences were investigated for example RF IC chips using different ESD protection structures. It was found that the ESD parasitic effects might have profound negative impacts on circuit performance due to both extra C_{ESD} and ESD-induced noises. It shows that novel compact ESD protection structures are desired to reduce such ESD-to-circuit influences while achieving adequate ESD protection, especially in RFIC applications.

References

(1) K. Narita, *et al*., *IEEE Trans. on Elect. Dev.*, pp. 1124, 1997.
(2) M-D Ker, *et al*, *IEEE JSSC, Vol. 32, No. 1, pp.38, Jan. 1997.*
(3) A. Wang, *et al*, in press, *IEEE Trans. Elect. Dev*. Vol 48 N4, 2001.
(4) A. Wang, *et al, Proc. IEEE CICC,* pp. 87, May 2000.

Table II Speed degradation *w.r.t.* original clock freq. due to C_{ESD}

ESD load	Original	ESD1	ESD2	ESD3
Single ESD load	0	-84.92%	-49.31%	-31.92%
	Improve-ment	⇒ +41.50% ⇒		
		⇒	+62.13%	⇒

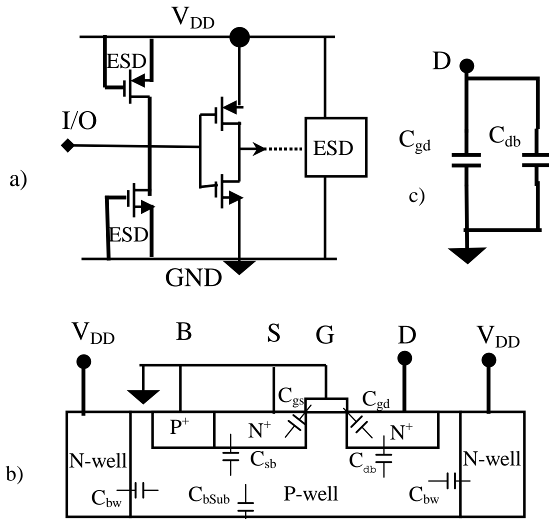

Fig. 1 ESD1: CMOS ESD protection: a) schematics, b) cross-section, and c) C_{ESD} model.

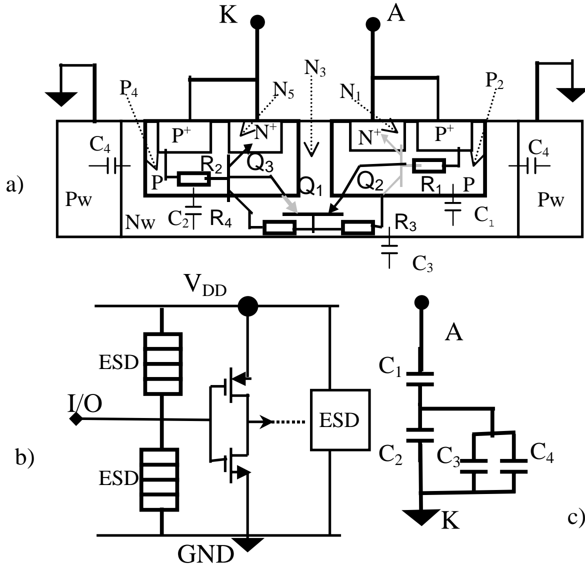

Fig. 2 ESD2: a new dual-direction ESD protection device.

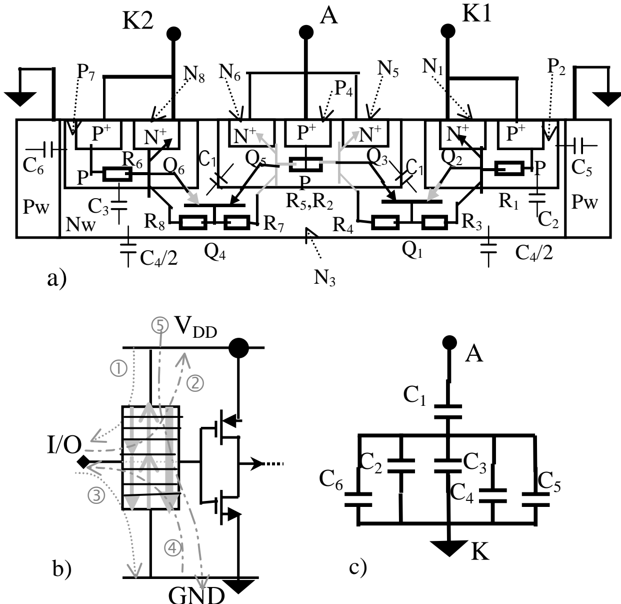

Fig3 ESD3: X-section, schematics and C_{ESD} model.

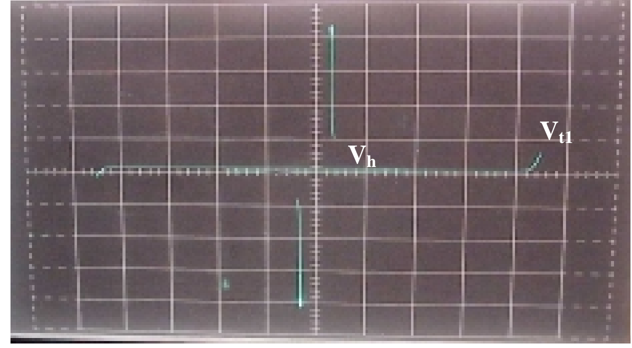

Fig. 4 Measured I-V curve of ESD3 device shows symmetry.

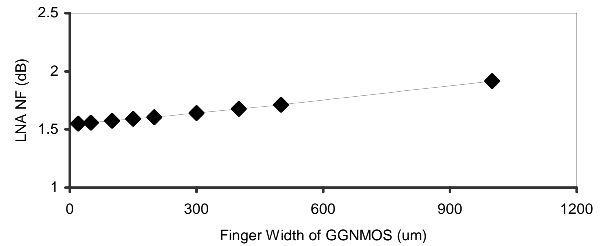

Fig. 5 NF versus GGNMOS size for the LNA.

Table I Data for ESD performance from simulation & measurement

ESD devices	Methods	Triggering V_{t1} (V)	Holding V_h (V)	R_{ON} (Ω)
ESD *1*	Simulation	14.68	6.92	~1.9
	C-tracer	12.56	6.48	-
	TLP	12.5	6.5	~1.02
ESD *2*	Simulation	23.32	1.58	0.73
	C-tracer	22.8	1.55	-
	TLP	21.75	2.96	1.4
ESD 3	Simulation	20.82	1.31	0.5
	C-tracer	22.5	1.5	-
	TLP	21.66	2.41	1.37

	ESD pass level		Triggering time t_I (nS)	Parasitic C_{ESD} (pF)
	Simulation	HBM Test		
ESD1,200μ	4KV	4KV	0.2	0.54
ESD2,50μ	4KV	4KV	0.18	0.09
ESD3,50μ	4KV	4KV	0.16	0.07

Table III Op Amp performance degradation due to C_{ESD} loads

Parameters	Original	ESD1	ESD2	ESD3
f_T (MHz)	126.3	-31.75%	-11.16%	-6.1%
		⇒ +64.85% ⇒		
		⇒	+80.86%	⇒
f_{-3dB} (KHz)	40.6	-7.4%	-2%	-2%
		⇒ +83.78% ⇒		
		⇒	+83.78%	⇒
Slew rate (V/us)	115.7	-30.34%	-7%	-5.5%
		⇒ +76.93% ⇒		
		⇒	+81.87%	⇒
t_{set} (nS, 1%)	9.38	-39.55%	-9.59%	-8%
		⇒ +75.98% ⇒		
		⇒	+79.77%	⇒

Table IV LNA noise figures using different ESD devices

ESD Structures	LNA NF (dB)
None	1.54
ESD1 (GGNMOS)	1.61
ESD2 (dual-direction)	1.55